[c2]

[c3]

[c4]

[c5]

[c6]

[c1] What is claimed is:

1.An shallow trench isolation (STI) method for semiconductor processes, the method comprising:

providing a substrate having a top surface;

forming a trench-patterned mask layer on the top surface exposing an unmasked trench region of the substrate, the mask layer comprising a pad oxide layer, and a silicon nitride layer formed on the pad oxide layer; etching the unmasked region of the substrate to form a trench in the substrate; depositing a high temperature oxide (HTO) film over the substrate, the HTO film covering the trench and the mask layer;

depositing a dielectric layer that fills the trench and covers the HTO film; planarizing the dielectric layer to expose the silicon nitride layer; and stripping the silicon nitride layer;

wherein the HTO film reinforces an interface between the dielectric layer and the substrate to prevent acid penetration and acid-corroded seams forming during the acid solution dipping process.

2.The method of claim 1 wherein the HTO film is formed by a low-pressure chemical vapor deposition (LPCVD) process, the LPCVD process utilizing a SiH  $_2$  Cl  $_2$  /N  $_2$  O gas system, a pressure of 0.4 Torr, and a temperature between 700  $^{\circ}$  C and 850  $^{\circ}$  C.

3. The method of claim 1 wherein the HTO film has a thickness between 50 and 250 angstroms.

4. The method of claim 1 wherein the dielectric layer is a high density plasma (HDP) oxide layer.

5. The method of claim 1 wherein before stripping the silicon nitride layer, the method further comprises performing a silicon oxide etching process to remove residual silicon oxide from the silicon nitride layer and to simultaneously etch the dielectric layer in the trench.

6.The method of claim 1 wherein the acid solution dipping process uses a

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diluted HF (DHF) solution.

[c7] 7.The method of claim 1 wherein a 160 ° C phosphoric acid solution is used to strip the silicon nitride layer.